UM10409

120 V high power factor CFL reference board using the UBA2014T

Rev. 1 — 12 October 2010 **User manual**

Document information

Info	Content
Keywords	UBA2014T, half-bridge CFL driver, high PF, triac dimmable
Abstract	This user manual describes the 120 V mains dimmable Compact Fluorescent Lamp (CFL) reference board with high power factor based on the UBA2014T

Revision history

Rev	Date	Description
v.1	20101012	initial version

Contact information

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1. Introduction

WARNING

Lethal voltage and fire ignition hazard

The non-insulated high voltages that are present when operating this product, constitute a risk of electric shock, personal injury, death and/or ignition of fire.

This product is intended for evaluation purposes only. It shall be operated in a designated test area by personnel qualified according to local requirements and labor laws to work with non-insulated mains voltages and high-voltage circuits. This product shall never be operated unattended.

Remark: Galvanic isolation of the mains phase using a variable transformer is always recommended. These devices can be recognized by the symbols shown in Figure 1.

a. Isolated b. Not isolated

Fig 1. Variac isolation symbols

The UBA2014T is a half-bridge driver IC used for electronically ballasted fluorescent lamps. In this application, it provides the drive function for two external MOSFETs and these supply power to the resonant tank circuit and Philips PL-C 4P 18 W CFL. The mains input is 120 V (RMS) ± 10 %.

The bus voltage is generated with a Power Factor Correction (PFC) or boost circuit which utilizes the same external MOSFETs. This PFC circuit, also known as a combined free running PFC, has a Power Factor (PF) greater than 95 %.

Dimming down to 10 % of lamp current (< 10 % lumens) is possible using a triac dimmer. A 120 V Lutron dimmer was used.

The application can be used with lamps in a laboratory environment and a protection circuit is included (outside the circular PCB). This protection circuit disables the operation of the UBA2014T when a lamp is not attached to the circuit. This circuit is not necessary when the application is included in a CFL housing.

Other protective circuits include:

- OverVoltage Protection (OVP) on bus voltage
- UnderVoltage LockOut (UVLO) which is not necessary in this application during deep dimming

2. Schematic Diagram

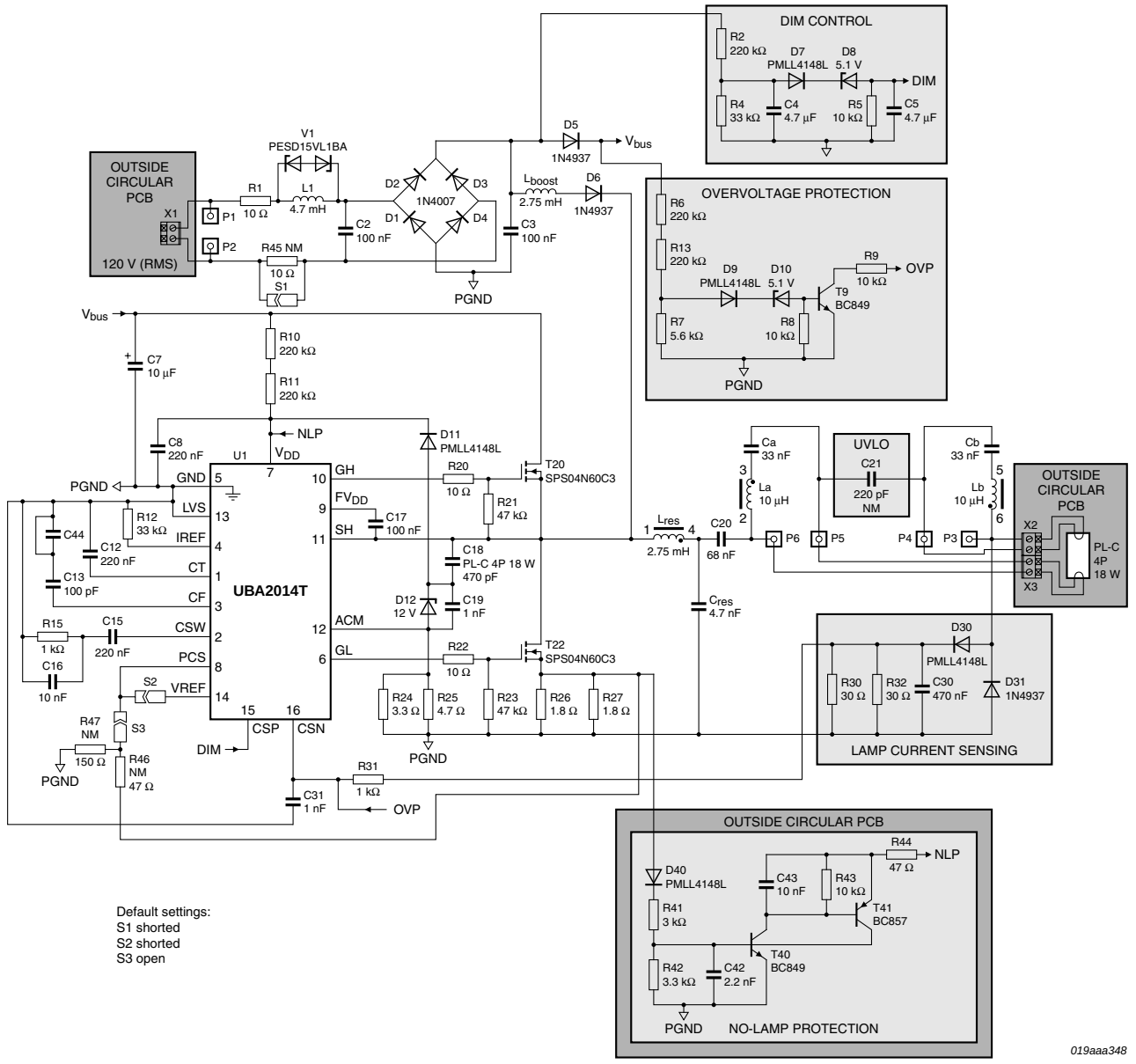
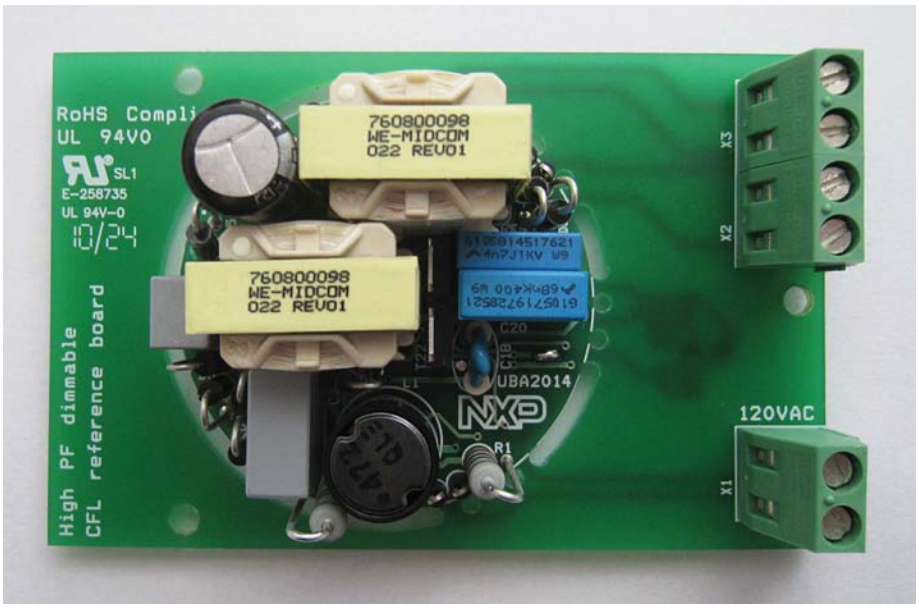


Fig 2. Schematic diagram high PF dimmable CFL using the UBA2014T

3. Specifications

This section describes the specifications used in the application; see Figure 2.



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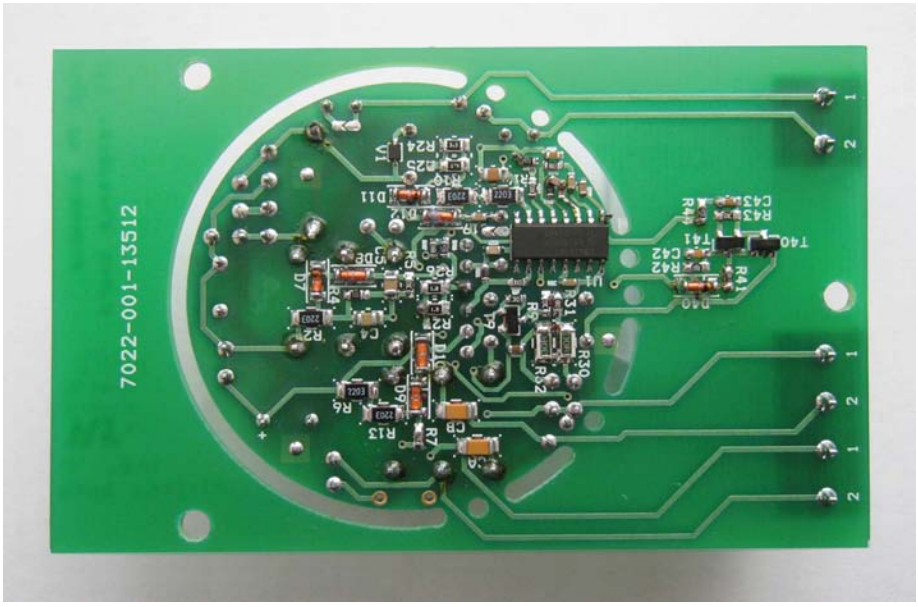
a. Top view



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b. Bottom view

Fig 3. High power factor 18 W CFL reference board using the UBA2014T

3.1 General

The UBA2014T high PF reference board powers a Philips PL-C 4P 18 W CFL. The reference board specifications are:

- Input voltage range: 120 V (RMS); ± 10 %; 50 Hz or 60 Hz
- Input power: 24 W at 120 V (RMS)
- Input current: 200 mA (RMS) for 120 V (RMS) mains input
- Dimmable to 10 % lamp current (< 10 % lumens) using triac dimmer
- Power factor > 0.95, efficiency (η) > 75 %
- Operating frequency 45 Hz; frequency range between 40 kHz and 100 kHz
- Preheat time: 1200 ms; preheat frequency can be set to f_{max} or variable using current sensing on the Low-Side (LS) MOSFET for Preheat Current Sensor (PCS) pin
- Rectangular board with connectors for mains and CFL and the possibility to break out the circular board (form factor = 45.5 mm) with additional connector pins for mains input and CFL on circular breakout board
- Board mounted fused resistor
- Complies with safety standards, EMI, RoHS, UL 1993 and UL 94V0

3.2 Protection circuits

- No-lamp protection by voltage sensing at LS MOSFET
- OverVoltage Protection (OVP) on the bus voltage (V_{bus})
- Optional UnderVoltage LockOut (UVLO)
- Capacitive mode protection

3.3 CFLs tested

- Philips PL-C 4P 18 W
- Philips PL-C 4P 23 W
- TCP 18 W
- Megaman 18 W
- Baishi 18 W

4. Reference board connections and bill of materials

4.1 Reference board connections

Direct board connections: connect 120 V (RMS) to terminal X1 and connect PL-C 4P 18 W CFL filaments to terminals X2 and X3, respectively.

Connection to the CFL's circular board is also possible: 120 V (RMS) is connected between P1 and P2. The CFL filaments are connected between P3/P4 and P5/P6, respectively.

If R45 is not needed, it must be short circuited to the mains return line using the solder connection S1. The default is with R45 as NM and S1 short circuited.

The preheat selection can be chosen as follows:

- When the PCS pin is set to VREF = 3 V using the solder connection S2, the preheat frequency is f_{max} (the default setting)
- The preheat frequency is set using the current sensing resistors R26/R27 which are connected between the LS MOSFET (T22) and ground. The voltage across the sensing resistor is attenuated by R46/R47 and supplied to the Preheat Current Sensor (PCS) pin using solder connection S3

4.2 Bill Of Materials (BOM) including the PL-C 4P 18 W CFL

Table 1. Reference board BOM including the PL-C 4P 18 W CFL

Reference	Description	Remarks	Value
Resistors			
R1	flameproof power metal film resistor	fused resistor; radial	10 Ω; 5 %; 2 W
R2	thick film resistor; 1206	SMD	220 kΩ; 1 %; 0.25 W
R4	thick film resistor; 0603	SMD	33 kΩ; 5 %; 0.1 W
R5	thick film resistor; 0603	SMD	10 kΩ; 5 %; 0.1 W
R6	thick film resistor; 1206	SMD	220 kΩ; 1 %; 0.25 W
R7	thick film resistor; 0603	SMD	5.6 kΩ; 5 %; 0.1 W
R8	thick film resistor; 0603	SMD	10 kΩ; 5 %; 0.1 W
R9	thick film resistor; 0603	SMD	10 kΩ; 5 %; 0.1 W
R10	thick film resistor; 1206	SMD	220 kΩ; 1 %; 0.25 W
R11	thick film resistor; 1206	SMD	220 kΩ; 1 %; 0.25 W
R12	thick film resistor; 0603	SMD	33 kΩ; 5 %; 0.1 W
R13	thick film resistor; 1206	SMD	220 kΩ; 1 %; 0.25 W
R15	thick film resistor; 0603	SMD	1 kΩ; 5 %; 0.1 W
R20	thick film resistor; 0603	SMD	10 Ω; 5 %; 0.1 W
R21	thick film resistor; 0603	SMD	47 kΩ; 5 %; 0.1 W
R22	thick film resistor; 0603	SMD	10 Ω; 5 %; 0.1 W
R23	thick film resistor; 0603	SMD	47 kΩ; 5 %; 0.1 W
R24	thick film resistor; 0805	SMD	3.3 Ω; 1 %; 0.25 W
R25	thick film resistor; 0805	SMD	4.7 Ω; 1 %; 0.25 W
R26	thick film resistor; 0805	SMD	1.8 Ω; 1 %; 0.25 W
R27	thick film resistor; 0805	SMD	1.8 Ω; 1 %; 0.25 W
R30	thick film resistor; 1206	SMD	30 Ω; 1 %; 0.25 W
R31	thick film resistor; 0603	SMD	1 kΩ; 5 %; 0.1 W
R32	thick film resistor; 1206	SMD	30 Ω; 1 %; 0.25 W
R41	thick film resistor; 0603	SMD	3 kΩ; 5 %; 0.1 W
R42	thick film resistor; 0603	SMD	3.3 kΩ; 5 %; 0.1 W
R43	thick film resistor; 0603	SMD	10 kΩ; 5 %; 0.1 W
R44	thick film resistor; 0603	SMD	47 Ω; 5 %; 0.1 W
R45	flameproof power metal film resistor	fused, radial (NM)	10 Ω; 5 %; 2 W
R46	thick film resistor; 0603	SMD (NM)	47 Ω; 5 %; 0.1 W
R47	thick film resistor; 0603	SMD (NM)	150 Ω; 5 %; 0.1 W

Table 1. Reference board BOM including the PL-C 4P 18 W CFL *...continued*

Reference	Description	Remarks	Value
Capacitors			
C2	polypropylene capacitor; class X2; lead spacing 10 mm	interference suppression capacitor; radial	100 nF; 20 %; 310 V (AC)
C3	metallized polyester film capacitor; lead spacing 5 mm	radial	100 nF; 5 %; 250 V
C4, C5	ceramic capacitor; X5R dielectric; 0805	SMD	4.7 μF; 10 %; 25 V
C7	aluminium electrolytic capacitor; lead spacing 5 mm	bus capacitor; radial	10 μF; 20 %; 450 V
C8	ceramic capacitor; X7R dielectric; 0805	SMD	220 nF; 5 %; 25 V
C12	ceramic capacitor; X7R dielectric; 0603	SMD	220 nF; 10 %; 10 V
C13	ceramic capacitor; NP0 dielectric; 0402	SMD	100 pF; 5 %; 50 V
C15	ceramic capacitor; X7R dielectric; 0603	SMD	220 nF; 10 %; 10 V
C16	ceramic capacitor; X7R dielectric; 0603	SMD	10 nF; 10 %; 50 V
C17	ceramic capacitor; X7R dielectric; 0603	SMD	100 nF; 10 %; 50 V
C18	ceramic capacitor; lead spacing 5 mm	dV/dt; radial	470 pF; 10 %; 1000 V
C19	ceramic capacitor; X7R dielectric; 0603	SMD	1 nF; 10 %; 50 V
C20	polyester capacitor; lead spacing 10 mm	DC blocking capacitor; radial	68 nF; 20 %; 400 V
C21	ceramic capacitor; lead spacing 5 mm	UVLO; radial (NM)	220 pF; 10 %; 1000 V
C30	ceramic capacitor; X5R dielectric; 0603	SMD	470 nF; 10 %; 16 V
C31	ceramic capacitor; X7R dielectric; 0603	SMD	1 nF; 10 %; 50 V
C42	ceramic capacitor; X7R dielectric; 0603	SMD	2.2 nF; 10 %; 50 V
C43	ceramic capacitor; X7R dielectric; 0603	SMD	10 nF; 10 %; 50 V
C44	ceramic capacitor; NP0 dielectric; 0402	SMD; shorted	-
Ca	ceramic capacitor; X7R dielectric; 1206	SMD	33 nF; 10 %; 50 V
Cb	ceramic capacitor; X7R dielectric; 1206	SMD	33 nF; 10 %; 50 V
C_{res}	metallized polypropylene film; lead spacing 10 mm	resonant capacitor; radial	4.7 nF; 5 %; 1000 V
Discrete, integrated components			
D1, D2, D3, D4	diode; standard; 1 KV; 1 A; DO-41	mains rectifier diode; radial; 1N4007	-
D5, D6	diode; fast recovery; 1 A; 600 V; DO-41	radial; 1N4937	-
D7	diode; high speed; SOD80C	SMD; PMLL4148L	-
D8	diode; 5.1 V Zener; SOD80C	SMD; BZV55-C5V1	-
D9	diode; high speed; SOD80C	SMD; PMLL4148L	-
D10	diode; 5.1 V Zener; SOD80C	SMD; BZV55-C5V1	-
D11	diode; high speed; SOD80C	SMD; PMLL4148L	-
D12	diode; 12 V Zener; SOD80C	SMD; BZV55-C12V	-
D30, D31	diode; fast recovery; 1 A; 600 V; DO-41	Radial; 1N4937	-
D40	diode; high speed; SOD80C	SMD; PMLL4148L	-
V1	bidirectional diode; SOD323	SMD, transient suppression; PESD15VL1BA	-
T9	NPN transistor; SOT23	SMD; BC849BL	-

Table 1. Reference board BOM including the PL-C 4P 18 W CFL *...continued*

Reference	Description	Remarks	Value
T20, T22	half-bridge MOSFETs; PG-TO251-3-11	SPS04N60C3	-
T40	NPN transistor; SOT23	SMD; BC849BL	-
T41	PNP transistor; SOT23	SMD; BC857	-
U1	half-bridge controller IC; SO16	UBA2014T	-
Inductors			
L1	ferrite inductor; 4.7 mH; 5R2; lead spacing 5 mm	filter inductor; radial	4.7 mH; 0.26 A; 10 %
L_{res}	ferrite inductor; EE20 core; bobbin UL-V0; TP4 core material	resonant inductor; Würth part nr. 76080098	-
	primary inductance		2.75 mH; 10 %
	secondary inductance for inductive mode heating	-	10 μH; 25 %
L_{boost}	ferrite inductor; EE20 core; bobbin UL-V0; TP4 core material; primary inductance	boost inductor; Würth part No. 76080098	2.75 mH; 10 %
X1	mains terminal connection outside circular PCB	5 mm; 2-way	-
X2	CFL filament 1 terminal connection outside circular PCB	5 mm, 2-way	-
X3	CFL filament 2 terminal connection outside circular PCB	5 mm, 2-way	-
P1, P2	isolated test pins for mains inputs inside circular PCB	PK100	-
P3, P4	isolated test pins for CFL filament 1 connection inside circular PCB	PK100	-
P5, P6	isolated test pins for CFL filament 2 connection inside circular PCB	PK100	-

5. Measurements

5.1 Preheat and Sum of Squares (SoS)

The hot to cold filament ratio (R_{ratio}) for the Philips PL-C 4P 18 W CFL was initially measured using a variable DC voltage source across the filament. Preheat is sufficient when R_{ratio} is approximately 5 : 1 (which is equivalent to a $V_{filament}$ of ±7.5 V).

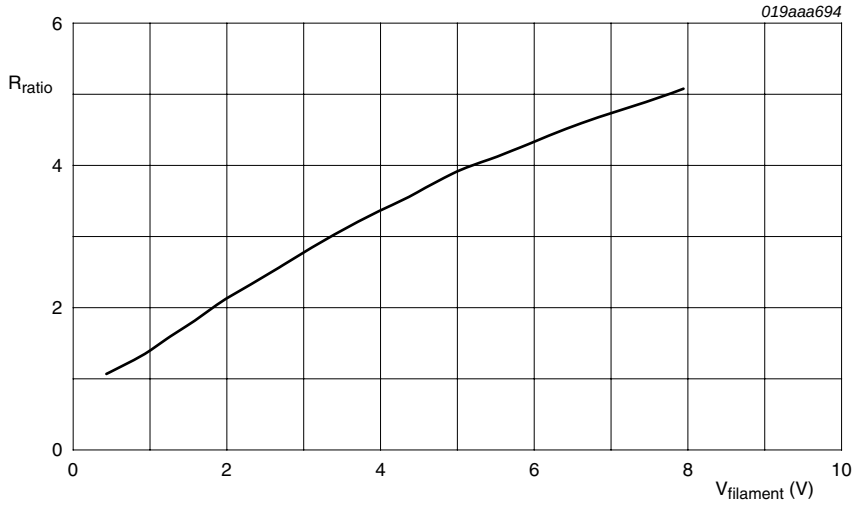


Fig 4. Ratio of hot to cold filament resistance against filament voltage for the PL-C 4P 18 W CFL

The preheat waveforms for the reference board are shown in Figure 5. $V_{filament}$ of 7.4 V (RMS) and $I_{filament}$ of 235 mA (RMS) are measured at the end of the preheat timer period giving a power supply to the filament of approximately 1.7 W.

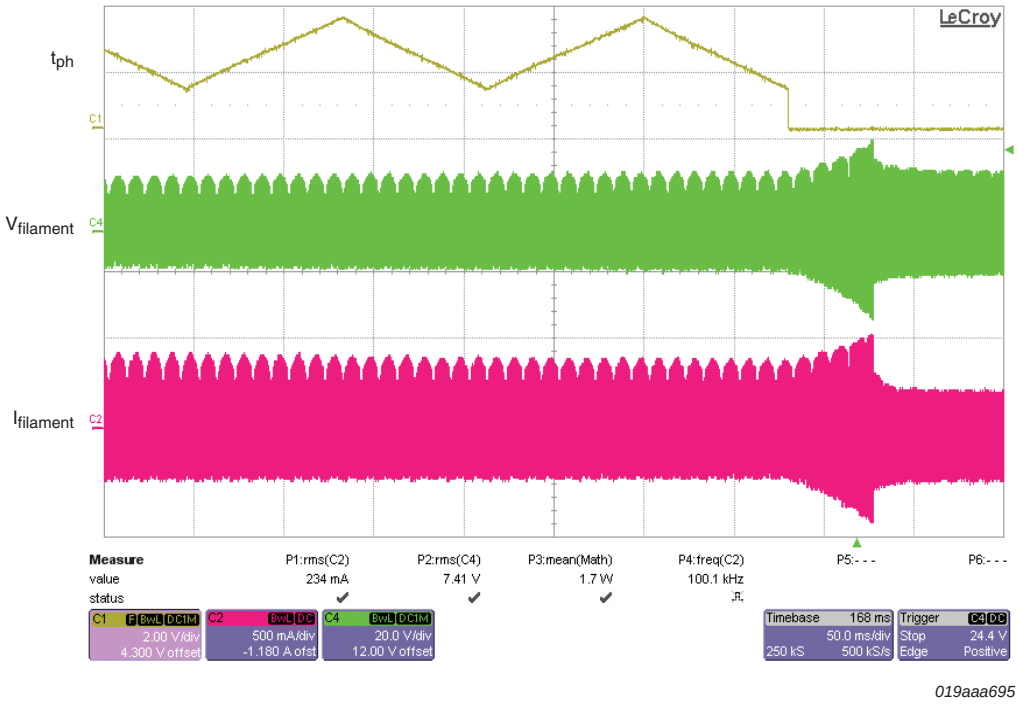


Fig 5. Preheat waveforms at end of preheat timer period for PL-C 4P 18 W CFL

The preheat frequency is set at 100 kHz by connecting pin VREF = 3 V to the PCS pin. The preheat time is set to 1.2 s using:

$$t_{ph} = 1.8 \times \left(\frac{C_{CT}}{330 \cdot 10^{-9}}\right)\left(\frac{R_{IREF}}{33 \cdot 10^{3}}\right) \quad (1)$$

where C_{CT} = 220 nF and R_{IREF} = 33 kΩ.

The preheat frequency can also be set by the current sensing resistors (see R26/R27 on Figure 2 on page 4) which are connected between the LS MOSFET and ground. The voltage across the sensing resistors is attenuated (R46/R47) and then supplied to the Preheat Current Sensor (PCS) pin using solder connection S3.

As an example, with R26/R27 = 1.8 Ω, R46 = 47 Ω and R47 open, the preheat frequency is approximately 70 kHz and the measured power supplied to the filaments is 3.2 W ($V_{filament}$ = 10 V (RMS) and $I_{filament}$ = 320 mA (RMS)) which is too high. In addition, the V_{bus} voltage exceeds 400 V (DC) (the rating of bus voltage) during the preheat time period.

The preheat frequency could be set higher by changing R26/R27 and the power to the filaments could be reduced by decreasing the preheat time. However, a preheat time of less than 0.4 s is not recommended.

Setting the preheat frequency to the maximum frequency for this application with the PL-C 4P 18 W CFL, is the default (and optimum) setting.

The Sum of Squares (SoS) gives a measure of the amount of heat that should be generated in the filaments to maintain the correct operating temperature. SoS is expressed by Equation 2:

$$SoS = I_{LH}^2 + I_{LL}^2 \quad (2)$$

where I_{LH} is the lead-high current or total current supplied to the filament and I_{LL} is the lead-low or filament heating current (see Figure 6).

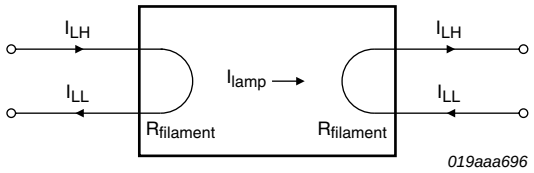
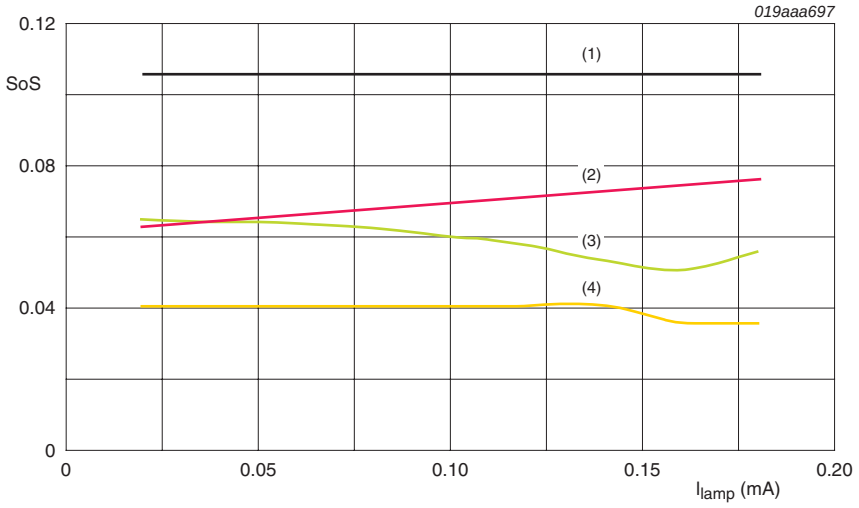


Fig 6. CFL electrode currents

The SoS curve shown in Figure 7 was measured over a dimming range of 20 mA to 180 mA lamp current.



(1) SoS maximum.
(2) SoS target.
(3) SoS measured.
(4) SoS minimum.

Fig 7. SoS for PL-C 4P 18 W

In Figure 8 and Figure 9, the waveforms for I_{LH} and I_{LL} are shown for both 180 mA and 20 mA lamp currents, measured with a current probe around the lead in wires. I_{lamp} is measured by taking both lead in wires through the current probe.

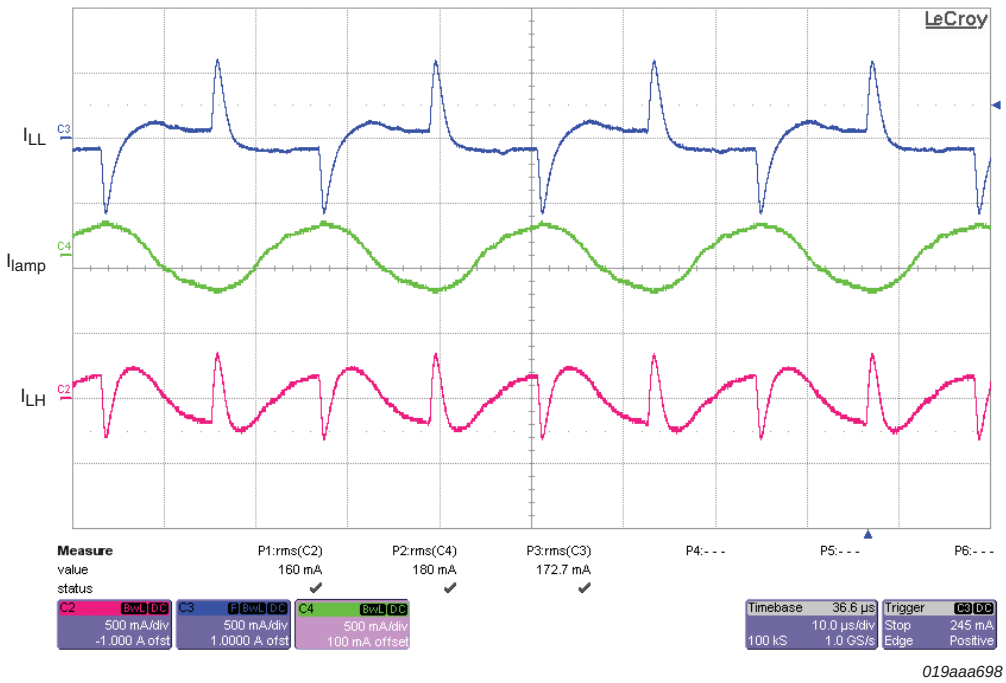


Fig 8. I_{LL}, I_{lamp} and I_{LH} for I_{lamp} = 180 mA

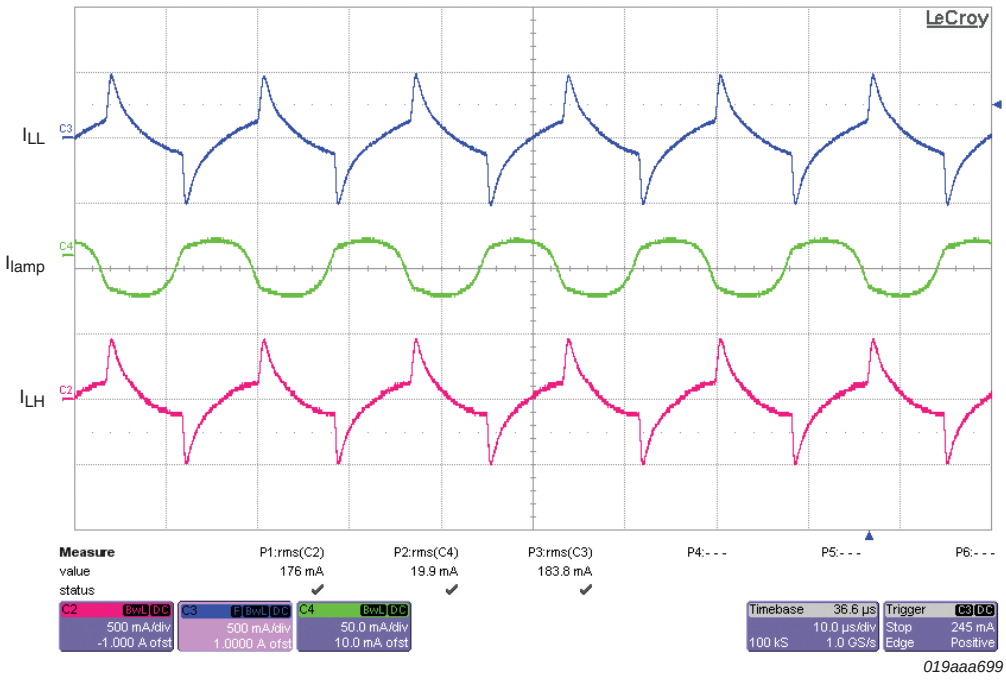


Fig 9. I_{LL}, I_{lamp} and I_{LH} for I_{lamp} = 20 mA

5.2 Preheat and lamp ignition

After the preheat timer period of 1.2 s, the frequency sweeps down from f_{max} to f_{min} where f_{min} and f_{max} are calculated using Equation 3 and Equation 4, respectively. Ignition occurs when the minimum lamp ignition voltage is exceeded.

$$f_{min} = 40.5 \times 10^3 \times \frac{100 \times 10^{-12}}{C_{CF}} \times \frac{33 \times 10^3}{R_{IREF}} \quad (3)$$

$$f_{max} = 2.5 \times f_{min} \quad (4)$$

where C_{CF} = 100 pF and R_{IREF} = 33 kΩ

The maximum preheat voltage must be less than the minimum lamp ignition voltage. In this application, the preheat frequency is set to maximum (100 kHz) during the preheat timer period which avoids overlapping of the maximum preheat voltage and minimum lamp ignition voltage will not occur. The maximum lamp ignition voltage must be reached before f_{min} is reached.

The measured ignition voltage at 25 °C is shown in Figure 10.

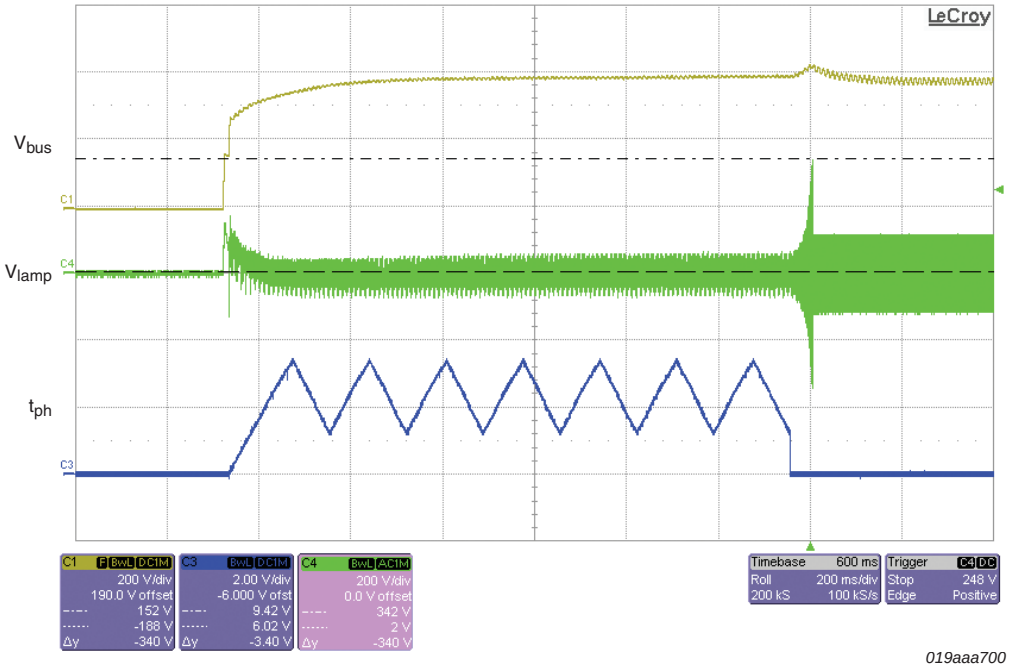


Fig 10. Preheat and lamp ignition waveforms

5.3 Efficiency, Power Factor (PF)

Using a mains input voltage of 120 V (RMS), the input current is 200 mA (RMS) and the input power is 24 W.

The losses are:

- Fused resistor 10 Ω is 0.4 W

- 4.7 mH EMI coil (R_{DC} = 5.2 Ω) is 0.5 W
- L_{boost} (R_{DC} = 9 Ω, I_{boost} = 260 mA (RMS)) is 0.6 W
- L_{res} (R_{DC} = 9 Ω, I_{Lres} = 275 mA (RMS)) is 0.7 W
- High-Side (HS) MOSFET ($R_{DS(on)}$ = 2.3 Ω, I_I = 275 mA (RMS)) is 0.2 W and Low-Side (LS) MOSFET ($R_{DS(on)}$ = 2.3 Ω, I_I = 360 mA (RMS)) is 0.3 W. The dissipation is 0.5 W for both MOSFETs. The waveforms shown in Figure 11 and Figure 12
- Each filament ($R_{filament}$ = 35 Ω, $I_{filament}$ = 175 mA) is 1.1 W, both filaments is 2.2 W

Total losses are approximately 5 W. The efficiency is $\frac{P_o}{P_{in}}$ = 80 %.

Table 2. Extra measurements for 120 V (±10%) for 50 Hz and 60Hz

Parameter	120 V (RMS)/50 Hz			120 V (RMS)/60 Hz		
	−10 (%)	nominal	+10% (%)	−10 (%)	nominal	+10% (%)
P_{in} (W)	21.5	26.5	30	21.5	25.5	30
P_{lamp} (W)	17.5	20.5	22.5	17.5	20.5	23
PF	0.99	0.99	0.99	0.99	0.99	0.99
CF	1.7	1.65	1.7	1.65	1.6	1.65
THD (%)	11	10.5	11	11.5	10	10.5
η (%)	81	77	75	81	80	77

5.4 MOSFET, boost and resonant inductor currents

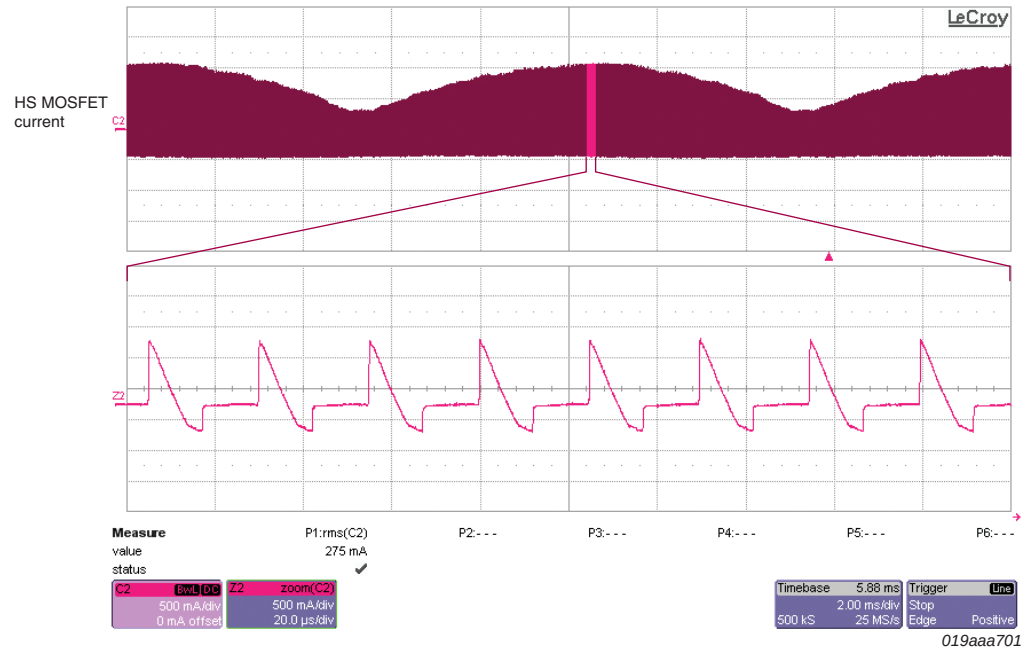


Fig 11. HS MOSFET current

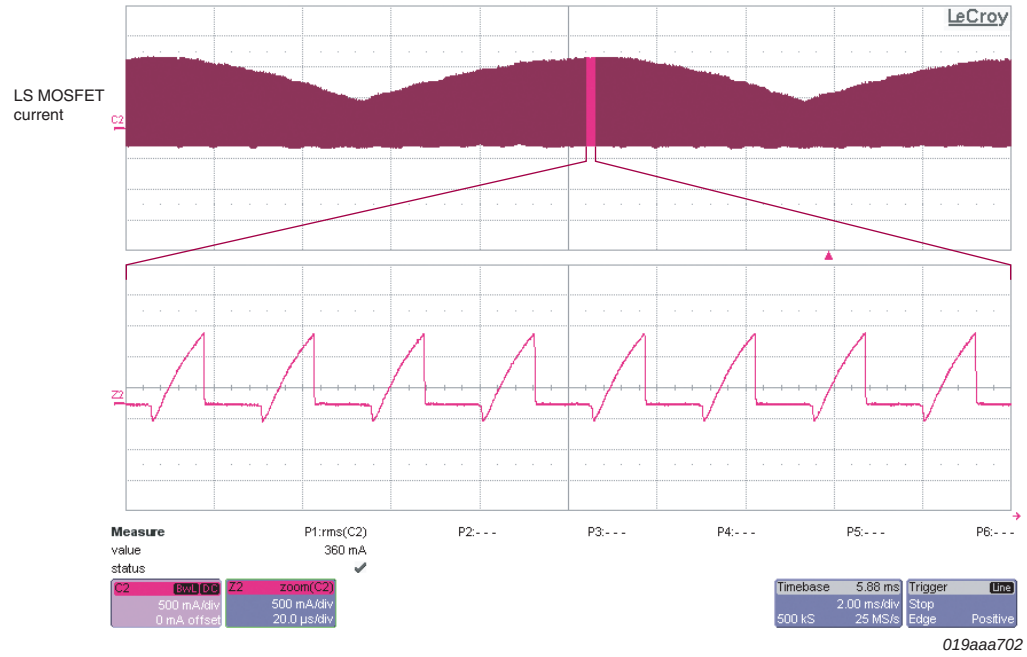


Fig 12. LS MOSFET current

The current in the HS MOSFET is the sum of the boost inductor and resonant inductor currents when the HS MOSFET is conducting.

Similarly, the current in the LS MOSFET is the sum of the boost inductor current and resonant inductor current when the LS MOSFET is conducting as shown in Figure 11 and Figure 12.

The sum of boost inductor and resonant inductor current which is I_{boost} + I_{Lres} is shown in Figure 13 and amounts to 460 mA (RMS) when measured over one cycle of the mains input.

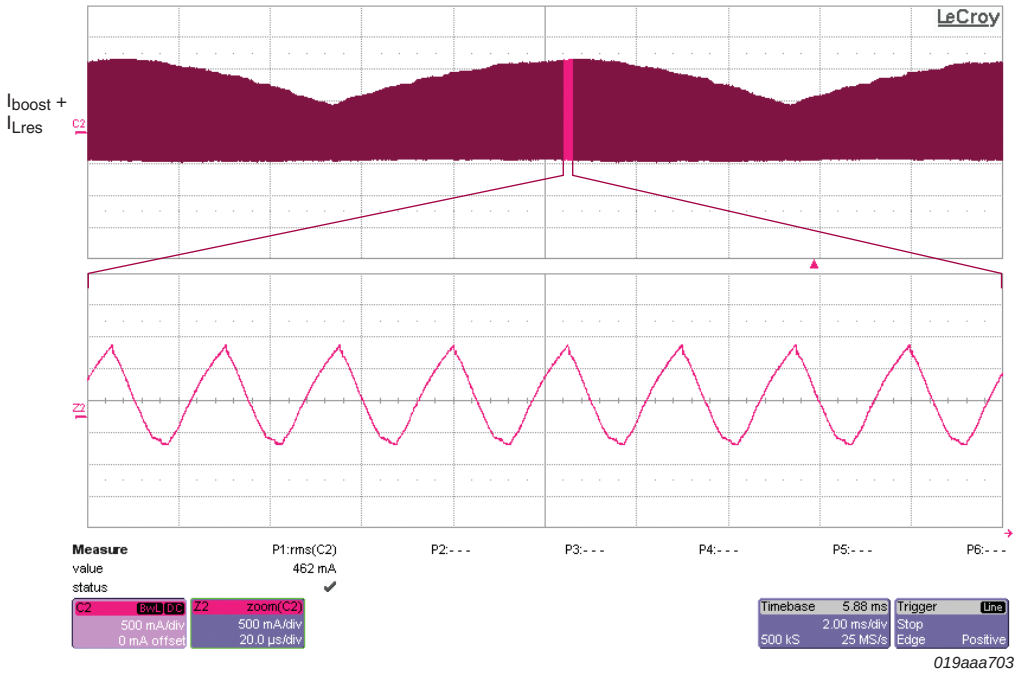


Fig 13. I_{boost} + I_{Lres}

5.5 Overvoltage protection circuit

It is necessary to have OverVoltage Protection (OVP) to protect the bus capacitance and MOSFETs from voltage transients greater than their rated values. The steady state voltage on the bus capacitance C7 = 10 µF (see Figure 2) is described by Equation 5:

$$V_P = \frac{120\sqrt{2}}{1-\delta} \quad (5)$$

where $P_{boost} = P_{lamp}$ and δ is a 50 % duty cycle.

If $P_{boost} > P_{lamp}$, as is in the case of deep dimming when there is a small load, the bus voltage can rise above the rated bus capacitance value. The OVP circuit is designed to start operating when the bus voltage is greater than an OVP level of approximately 400 V. The OVP circuit then reduces the CSN pin voltage by 10 % (set by R9 in Figure 2) and the half-bridge frequency decreases implying that P_{lamp} increases and the bus voltage decreases under the OVP level.

When testing with different dimmers and for fast transient steps in the triac dimmer, the bus voltage did not rise above 400 V (DC).

However, the OVP circuit was tested by supplying an external step on the bus voltage to the OVP circuit from 0 V (DC) to 410 V (DC) and at approximately 400 V (DC) the voltage on the CSN pin decreased by 10 %. The waveforms of the bus voltage to the OVP circuit and voltage at the CSN pin are shown in Figure 14.

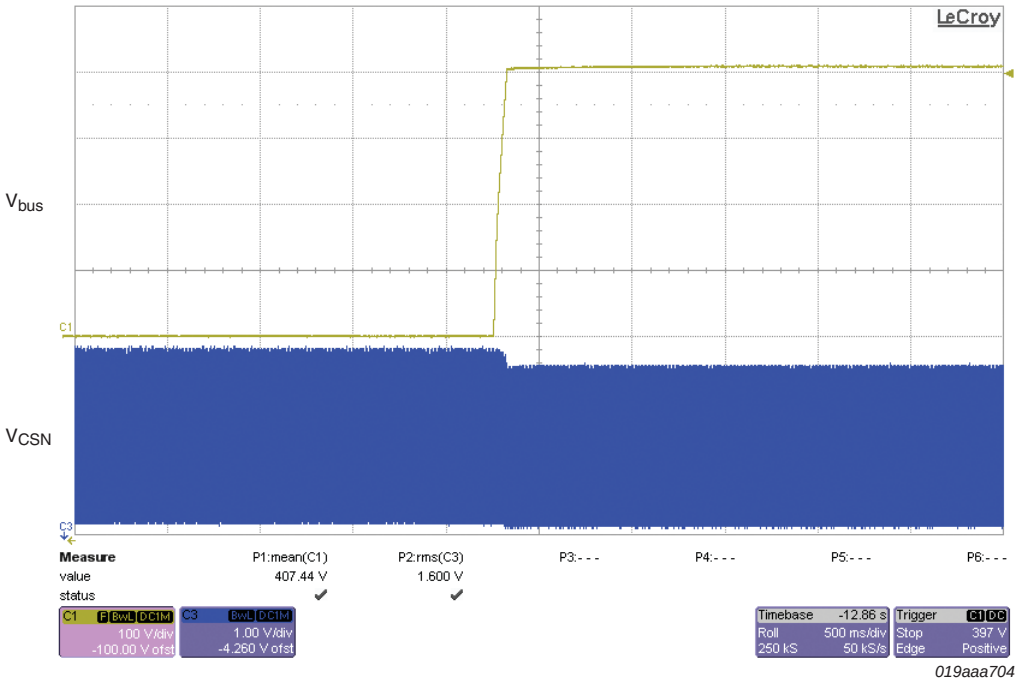


Fig 14. OVP circuit test with bus voltage and voltage at CSP pin

5.6 No-lamp detection

When a lamp is not connected, the voltage across the resonant capacitor continues to rise as the frequency sweeps down after preheat. The current in the MOSFETs can become excessive causing eventual damage to the internal drivers in the UBA2014T and external MOSFETs.

The no-lamp detection/latch circuit monitors the voltage (V_{SENSE}) across the sense resistor (parallel combination of R26/R27 which is 0.9 Ω) and thus, the current through the LS MOSFET. The resistors R26 and R27 are connected between the LS MOSFET source and ground as shown in Figure 2. When no-lamp is connected this voltage rises as the frequency sweeps down after the preheat time. The no-lamp detection/latch circuit is designed (using R41, R42 and R26, R27 in Figure 2) to trigger the latch and pull V_{DD} to ground when the voltage across the lamp terminals exceeds approximately 2.5 times the ignition voltage.

The relevant waveforms are shown in Figure 15.

The no-lamp protection circuit is reset by removing the mains voltage.

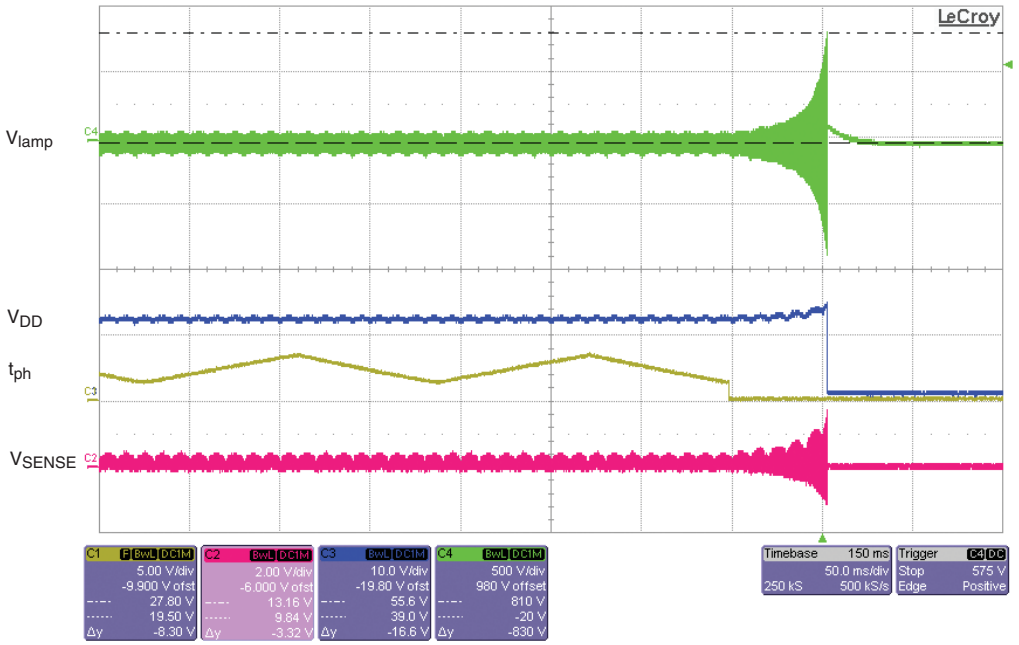


Fig 15. Waveforms for V_{lamp}, V_{DD}, preheat time (t_{ph}) and V_{SENSE} (across sense resistors R26, R27)

5.7 EMI prescan measurements

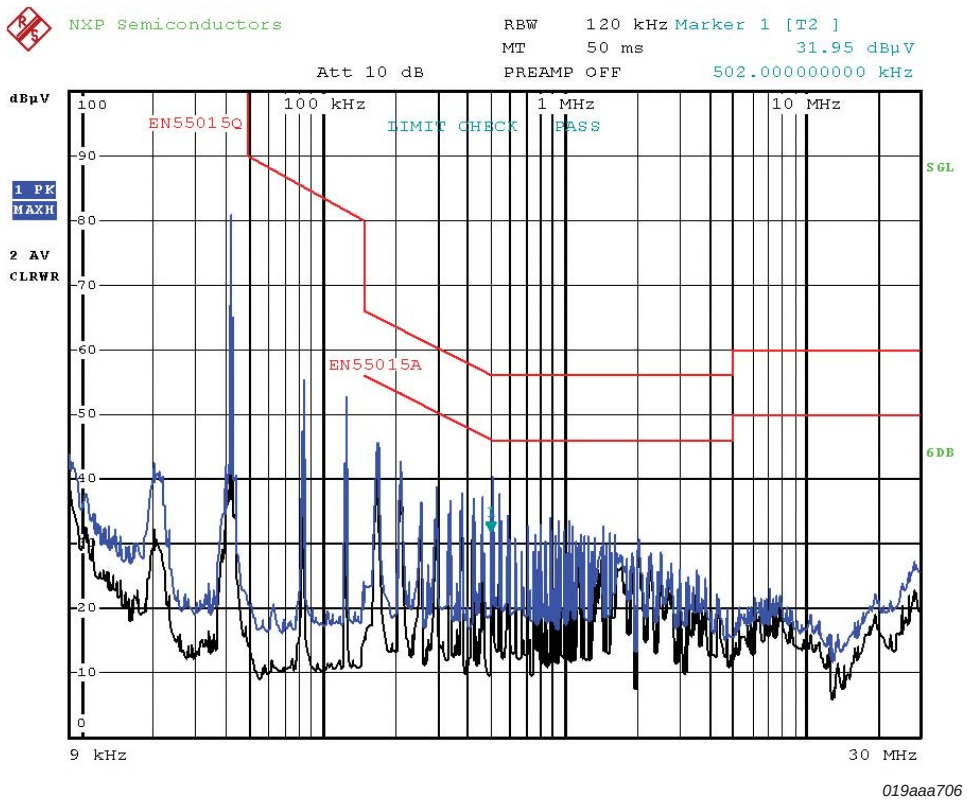


Fig 16. EN55015Q and EN55015A conducted EMI measurements, 120 V, 60 Hz mains input

6. Inductor specification

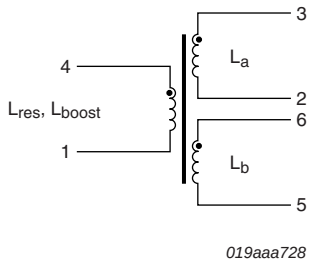


Fig 17. Inductor schematic

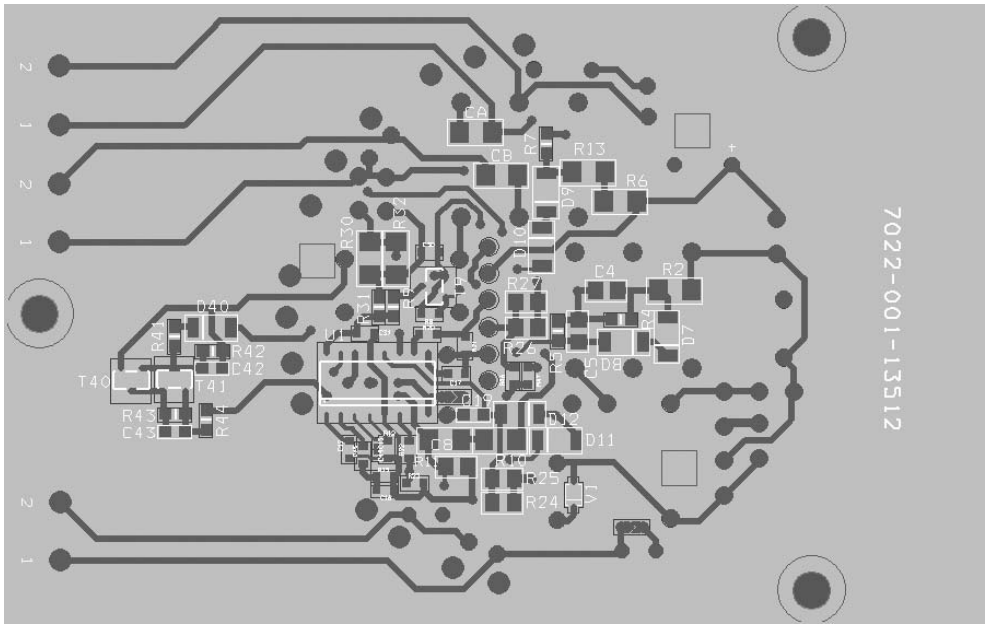
Table 3. Electrical characteristics

Parameter	Inductance (mH)	Resistance (Ω)	Rated current (A)	Saturation current (A)
L_{res}	2.75 ±10 %	9	0.35	1.1
L_a, L_b	0.010 ±25 %	0.495	-	-
L_{boost}	2.7 5 ±10 %	9	0.35	1.1

7. PCB layout

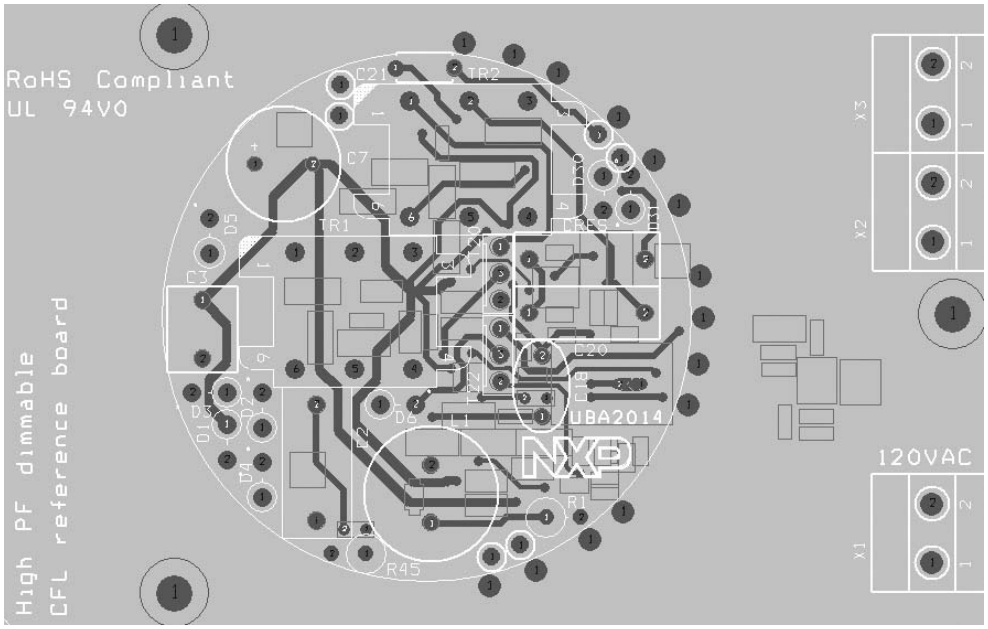
The following should be taken into account for the PCB layout:

- Separate ground of bridge rectifier back to bus capacitance (C7) ground (PGND in Figure 2)
- Components on pins 1 to 4 close to the UBA2014T and their grounding should be closely routed back to pin 5 of the UBA2014T (GND in Figure 2)
- Pin 5 (GND) of the UBA2014T should be routed back separately to C7 ground to minimize influence of PGND on GND
- Inductors L_{boost}, L_{res} and L1 should not be placed near the UBA2014T to minimize the magnetic field interference to the IC
- The grounding of both the lamp current sensing circuit and dim control should be connected closely together with separate routing back to bus capacitance (C7) ground (PGND)
- External MOSFETs close to L_{res}, L_{boost} and bus capacitance so as to have small current loops
- The half-bridge node tracks to L_{res}, L_{boost} and pin 11 of UBA2014T should be short to minimize interference from the half-bridge dV/dt voltage
- Sense resistors (R26/R27) ground routed back separately to C7 ground (PGND)
- ACM sense resistors (R24/R25) close to pin 12 (ACM) of UBA2014T and their grounding routed back separately to C7 ground (PGND)



019aaa710

Fig 18. PCB bottom layer



019aaa709

Fig 19. PCB top layer

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9. Figures

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